ABSTRACT OF THE DISCLOSURE

A ferroelectric memory comprising a plurality of memory cells each including a ferroelectric capacitor and a switch transistor, and operating in a test mode in which, after polarized data is written into the memory cell by applying a first electric potential difference between both electrodes of ferroelectric capacitors of the plurality of memory cells, and before reading of the polarized data from the memory cells is carried out, a second electric potential difference smaller than the first electric potential difference is applied between both the electrodes of the ferroelectric capacitors in a direction opposite to that at the time of writing the polarized data.